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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/530,495	04/06/2005	Ramanathan Sethuraman	NL 020975	4791
24737	7590	10/04/2006	EXAMINER	
PHILIPS INTELLECTUAL PROPERTY & STANDARDS				FONG, VINCENT
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BRIARCLIFF MANOR, NY 10510				
		ART UNIT		PAPER NUMBER
		2112		

DATE MAILED: 10/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/530,495	SETHURAMAN ET AL.
	Examiner	Art Unit
	Vincent Fong	2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 12 January 2006.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-17 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-17 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 06 April 2005 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>01-12-2006</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office Action is in response to the application filed on 04-06-2005.

Claims 1-17 are pending and have been examined.

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. EU 02079219.8, filed on 04-06-2005.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 01-12-2006 is being considered by the examiner.

Drawings

3. The drawings are objected to because Element 26 in Figure 2 is shown outside of Element 12, which contradict to the description in the Specification (Page 5 Lines 6-8). In the Specification, it is stated that Element 12 'contains' Element 26. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be

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canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency.

Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

- (a) TITLE OF THE INVENTION.
- (b) CROSS-REFERENCE TO RELATED APPLICATIONS.
- (c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
- (d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
- (e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
- (f) BACKGROUND OF THE INVENTION.
 - (1) Field of the Invention.
 - (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
- (g) BRIEF SUMMARY OF THE INVENTION.

(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

4. The disclosure is objected to because of the following informalities:
5. Page 5 Lines 6-8 state that Element 12 contains Element 26, which contradict to the drawing in Figure 2.
6. Page 5 Lines 26 and 30, the first one of the memory units should be numbered as 20.
7. Page 11 Line 9, it should be 'or' by profiling instead of 'of' by profiling.
Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
9. Claim 13 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In specification that is no mention of any part to facilitate the execution of variable length

instructions by the execution unit. In addition there is no mention of any part to decode variable length instruction part from partly the same location in the instruction word. The disclosed material is enough to enable one skilled in the art to which it pertains to make and/or use the invention.

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. From the claim the terms "relatively shorter" and "relatively longer" are indefinite. For examination the terms are interpreted as "shorter" and "longer" respectively.

12. Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. From the claim it is unclear that while first and second instructions are different in length that whether they represent the same operation to the execution unit.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. Claims 1-5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fisher et al.(USPN 6026479, hereinafter Fisher) in view of Barry et al.(USPN 6735690, hereinafter Barry).

As per Claim 1, Fisher discloses a data processing apparatus (Abstract Line 1, Column 1 lines 10-13), the apparatus comprising:

An instruction memory address generation circuit for outputting an instruction address, Fisher discloses instruction cache includes address decode to decode instruction address to select corresponding line from the cache (Column 8 lines 41-65), therefore it is inherent that an instruction memory address generation circuit exists in Fisher's invention for outputting an instruction to the decoder in the cache.

An instruction memory system (Figure 2 Element 120,122, Column 5 lines 25-31, 38-40) arranged to output an instruction word (Column 5 lines 25-31, 38-40) addressed by the instruction address, Fisher discloses using the instruction address bits to perform tag check in the cache to output the correspond line to output (Column 8 lines 60-65).

An instruction unit (Figure 2 Element 150A-D as a whole, Column 2 Line 63-66), arranged to process a plurality of instruction from the instruction word (Column 3 Line 55 – Column 4 Line 5) in parallel (Abstract lines 1-10).

And Fisher discloses a way to control how the instruction execution unit parallelizes processing of the instruction word from the instruction word by supplying the CPU an interrupt(Column 6 lines 38-47).

Fisher does not disclose an detection unit to control the way execution unit parallelizes processing of the instruction depending on the detected range of instruction address. However, Barry discloses the above limitations (Column 1 lines 44-45), where “generalized eventpoint mechanism” is the detection unit because it allows the user to define a group of event (includes if an instruction address occurred) to detect and define a group of action (includes generating an interrupt) to take in the event of such detections (Abstract lines 4 to 15). Barry’s invention include multiple register to define multiple event(Figure 4 Element 410, Column 8 lines 15-20), also it is possible to specify a range of instruction address to generate interrupt by using mask register (Column 25 lines 5 –12).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on Fisher’s inventions to incorporate Barry’s inventions so the detection unit disclosed by Barry will detect the range of instruction address and generate interrupt according to switch between high/low ILP mode in Fisher’s invention. One of ordinary skill in the art would be motivated to include a detection unit (Barry Column 1 line 44-45) which is providing a common and flexible design for all different type of functions often needed by the processor (Column 2 lines 4-13, 33-41).

As per claim 2, the rejection of claim 1 is incorporated and Fisher further discloses: Instruction memory system (Figure 2 Element 120,122, Column 5 lines 25-31, 38-40) is arranged to adjust a width of the instruction word that determines a number of

instruction from the instruction word that is processed in parallel (Column 5 line 62-67 and Column 6 line 55 –63) depends on the interrupt received that switch between high/low ILP mode (Column 6 line 38-47).

Fisher does not disclose such adjustment of width dependent on detected instruction range.

However, Barry discloses the above limitations. See rejection of Claim 1.

As per claim 3, the rejection of claim 1 is incorporated and Fisher further discloses:

The instruction execution unit (Figure 2 Element 150A-D as a whole, Column 2 Line 63-66) comprises a plurality of functional unit (Figure 2 Element 150A,B,C,D, Column 2 Line 63-66), the instruction execution unit being arranged to select a subset of the functional unit that is available for processing the instructions (Column 7 lines 15 –36) depend on the interrupt received that switch between high/low ILP mode(Column 6 line 38-47). Depending on the ILP mode, some of the execution unit would be dormant and unavailable to execute instructions (Column 7 lines 15 –36).

Fisher does not disclose the selection based on detected range.

However, Barry discloses the above limitations. See rejection of Claim 1.

As per claim 4, the rejection of claim 1 is incorporated and Fisher further discloses:

The instruction execution unit (Figure 2 Element 150A-D as a whole, Column 2 Line 63-66) comprises a plurality of functional unit (Figure 2 Element 150A,B,C,D, Column 2 Line 63-66), the instruction execution unit being arranged to select whether functional

units or groups of functional unit from a set of functional unit each receive respective instructions from the instruction word, or receive a shared instruction from the instruction word (Column 5 lines 63-67, Column 6 lines 55-56) depend on the interrupt received that switch between high/low ILP mode(Column 6 line 38-47). In high ILP mode, execution unit 150 A-D will all received instruction from the instruction word, while in low ILP mode, only execution unit 150 D will receive instruction from instruction word (Column 5 lines 63-67, Column 6 lines 55-56).

Fisher does not disclose the selection based on detected range.

However, Barry discloses the above limitations. See rejection of Claim 1.

As per claim 5, the rejection of claim 2 is incorporated and Fisher further discloses: The instruction memory comprises a first memory unit (Figure 2 Element 120) and a second memory unit (Figure 2 Element 122), providing storage with a first (Column 5 lines 26-33) and second (Column 3 lines 2-3) unit of width of addressable memory locations for instruction words of different lengths with addresses in a first and second range respectively (Column 7 Line 15-26), the first and second unit of width being mutually different. In Fisher's invention the first memory unit store multiple execution unit instruction as an instruction word, while the second memory unit store single execution unit instruction as an instruction word therefore they are instruction words of different lengths. Also the compiled code are store into first or second memory unit according to their ILP, therefore it is inherent that the first and second memory unit with address in a first and second range respectively.

As per claim 7, the rejection of claim 5 is incorporated and Fisher further discloses:

A memory mapping unit arranged to map the instruction address (Column 7 lines 26-32) onto the first memory unit (Figure 2 Element 120) or the second memory unit (Figure 2 Element 122) dependent on the interrupt received that switch between high/low ILP mode (Column 6 line 38-47). In high (low) ILP mode, the first memory unit (second memory unit) will remain active and memory access will be mapped to the active unit.

Fisher does not disclose such mapping dependent on detected instruction range.

However, Barry discloses the above limitations. See rejection of Claim 1.

15. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fisher in view of Barry as applied to claim 5 above, and further in view of Lilja et al. (Exploiting the parallelism available in loops, IEEE Computer, February 1994)(hereinafter Lilja).

As per claim 6, the rejection of claim 5 is incorporated and Fisher further discloses:

Longer instruction words (Column 5 lines 26-33) with higher ILP of the program being stored in the first memory unit (Column 7 lines 17-21), shorter instruction words (Column 3 lines 2-3) with lower ILP of the program being stored in the second memory unit (Column 7 lines 22-26), the first unit of width being larger than the second unit of width (Column 5 lines 26-33, Column 3 lines 2-3).

Fisher does not disclose what type of code would have high/low ILP.

However, Lilja discloses that loops comprise larger portion of parallelism (Page 1 lines 15-16).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on Fisher's inventions to incorporate Lilja's disclosure. One of ordinary skill in the art would be motivated to exploit loop's parallelism by placing them into the first memory unit due to the abundance of compiling technique to increase the ILP of loop during execution (Page 1 lines 23-26).

As per claim 14, the rejection of claim 1 is incorporated and Fisher further discloses:

A method of programming a data processing apparatus, method comprising:

Generating a program of machine instructions for the apparatus (Column 7 lines 15-37);

Identifying high ILP portion of the program (Column 7 lines 15-37);

Loading the program into instruction memory system, so that instructions with high ILP are loaded at memory location with instruction address in a range of address for which the apparatus provides a higher degree of parallelism than another range of addresses(Column 7 lines 15-37).

Fisher does not disclose what type of code would have high/low ILP.

However, Lilja discloses the above limitations. See rejection of Claim 6.

16. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fisher in view of Barry as applied to claim 5 above, and further in view of Maiyuran et al. (US PGPub 2002/0129201 A1, hereinafter Maiyuran).

As per claim 8, the rejection of claim 5 is incorporated and Fisher further discloses:

The instruction memory system(Figure 3 Element 120,122) is arranged to power down (Column 7 lines 15-36, Column 8 lines 21-25) the first memory unit(Figure 3 Element 120) dependent on the interrupt received that switch between high/low ILP mode (Column 6 line 38-47).

Fisher does not disclose that powering down unit dependent on the detected range of instruction address and powering down unit by disable supply of clock signal to the unit.

However, Barry discloses a “generalized eventpoint mechanism” that is the detection unit because it allows the user to define a group of event (includes if an instruction address occurred) to detect and define a group of action (includes generating an interrupt) to take in the event of such detections (Abstract lines 4 to 15). Barry’s invention include multiple register to define multiple event(Figure 4 Element 410, Column 8 lines 15-20), also it is possible to specify a range of instruction address to generate interrupt by using mask register (Column 25 lines 5 –12).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on Fisher’s inventions to incorporate Barry’s inventions so the detection unit disclose by Barry will detect the range of instruction address and generate interrupt according to switch between high/low ILP mode in Fisher’s invention to power down unit dependent on detected

range. One of ordinary skill in the art would be motivated to include a detection unit (Barry Column 1 line 44-45) which is providing a common and flexible design for all different type of functions often needed by the processor (Column 2 lines 4-13, 33-41).

Barry does not disclose powering down unit by disable supply of clock signal.

Further, Maiyuran discloses memory system that power down module depending on the instruction that is processing by the memory system (Abstract lines 2-5). The determination of unit power down depends on the address of the instruction in process (Paragraph 0015). The system power down the module of memory by disable the clock signal to the memory module (Paragraph 0028).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on the combination of Fisher and Barry's inventions to incorporate Maiyuran's inventions so the system of Fisher and Barry will power down dormant memory unit by disable the supply of clock signals. One of ordinary skill in the art would be motivated to achieve power saving by powering down unused memory module on a instruction by instruction basis (Paragraph 0013).

As per claim 9, the rejection of claim 5 is incorporated and Fisher further discloses: The instruction memory system(Figure 3 Element 120,122) is arrange to power down (Column 7 lines 15-36, 62-67, Column 8 lines 1-7, 21-25) all memory unit but the memory with the requested instruction dependent on the interrupt received that switch between high/low ILP mode (Column 6 line 38-47).

Fisher does not disclose that powering down unit dependent on the detected range of instruction address and powering down unit by disable supply of clock signal to the unit. However, Barry discloses a detection unit (Column 1 lines 44-45). See rejection of Claim 8.

Barry does not disclose that powering down unit by disable supply of clock signal.

Further, Maiyuran discloses the above limitations. See rejection of Claim 8.

17. Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fisher in view of Barry as applied to claim 2 above, and further in view of Sanches et al. (US PG Pub 2002/0116596 A1, hereinafter Sanches).

As per claim 10, the rejection of claim 2 is incorporated and Fisher further discloses: Instruction memory system (Figure 2 Element 120,122, Column 5 lines 25-31, 38-40) comprises a plurality of memory units, each arranged to be responsive (Column 7 lines 15-36, 62-67, Column 8 lines 1-7, 21-25) dependent on the interrupt that switch between high/low ILP mode (Column 6 line 38-47).

Fisher does not disclose a memory system responsive to instruction address range and it doesn't arrange the system instruction word as a combination from memory units. However, Barry discloses a "generalized eventpoint mechanism" that is the detection unit because it allows the user to define a group of event (includes if an instruction address occurred) to detect and define a group of action (includes generating an interrupt) to take in the event of such detections (Abstract lines 4 to 15). Barry's

invention include multiple register to define multiple event(Figure 4 Element 410, Column 8 lines 15-20), also it is possible to specify a range of instruction address to generate interrupt by using mask register (Column 25 lines 5 –12).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on Fisher's inventions to incorporate Barry's inventions so the detection unit disclose by Barry will detect the range of instruction address and generate interrupt according to switch between high/low ILP mode in Fisher's invention. One of ordinary skill in the art would be motivated to include a detection unit (Barry Column 1 line 44-45) which is providing a common and flexible design for all different type of functions often needed by the processor (Column 2 lines 4-13, 33-41).

Barry does not disclose arrangement of the system instruction word as a combination from memory units.

Further, Sanches discloses a instruction memory system that comprises a plurality of memory units each responsive to some instruction address (Abstract lines 3-6). The instruction allow overlap of address range (Paragraph 0042, Table 2), all memory unit can response to the same memory address (overlap) while contain only part of the data for the address. The system is arranged to supply instruction word as a combination of instructions from those memory units (Abstract lines 8-13Paragraph 0028, 00042).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on the combination of Fisher and Barry's inventions to incorporate Sanches's inventions. One of ordinary skill in the art

would be motivated to save memory space by excluding NOP from the code (Paragraph 0015).

As per claim 12, the rejection of claim 10 is incorporated and Fisher further discloses:

The instruction execution unit (Figure 2 Element 150A-D as a whole, Column 2 Line 63-66) comprises groups of one or more functional unit (Figure 2 Element 150A,B,C,D, Column 2 Line 63-66), each group being coupled to a respective predetermined one of the memory unit(Column 5 lines 26-53, Column 7 lines 14-36), for receiving instructions from the instruction words depend on the interrupt received that switch between high/low ILP mode(Column 6 line 38-47).

Fisher does not disclose the coupling based on detected range.

However, Barry discloses a detection unit. See rejection of Claim 10.

18. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fisher in view of Barry in further view of Sanches as applied to claim 10 above, and further in view of Maiyuran.

As per claim 11, the rejection of claim 10 is incorporated and Fisher further discloses:
The instruction memory system (Figure 3 Element 120,122) is arrange to power down (Column 7 lines 15-36, 62-67, Column 8 lines 1-7, 21-25) at least one memory unit when instruction address does not fall on that memory dependent on the interrupt received that switch between high/low ILP mode (Column 6 line 38-47).

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Fisher does not disclose that powering down unit dependent on the detected range of instruction address and powering down unit by disable supply of clock signal to the unit.

Barry discloses a detection unit. See rejection of Claim 8.

Barry does not disclose that powering down unit by disable supply of clock signal.

Further, Maiyuran discloses the above limitations. See rejection of Claim 8.

19. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fisher in view of Barry as applied to claim 3 above, and further in view of Takayama et al. (USPN 6085306, hereinafter Takayama).

As per claim 13, the rejection of claim 3 is incorporated and Fisher further discloses:

A instruction execution unit ((Figure 2 Element 150A-D as a whole, Column 2 Line 63-66) execute instruction dependent on the interrupt received that switch between high/low ILP mode (Column 6 line 38-47). Only one instruction will be able to execute at one cycle in low ILP mode while multiple instructions will be able to execute at one cycle in high ILP mode. Thus in low ILP mode, the first instruction in the word will be issued in the cycle, while in high ILP mode all instructions in the word will be issued in the cycle.

Fisher does not disclose instruction execution dependent on the instruction address, instruction execution unit capable of processing instruction with different length and derived two instructions with different length at least partly from a same location.

However, Barry discloses a detection unit. See rejection of Claim 1.

Barry does not disclose instruction execution unit capable of processing instruction with different length and derived two instructions with different length at least partly from a same location.

Further, Takayama discloses a VILW processor (Column 1 lines 55-61) that able to process instructions with two different length (Figure 2A, Figure 2C Element A, Column 4 lines 44-49). Element A in Figure 2C embedded two instructions in a word, which the branch instruction consists of 16 bits and the second instruction consists of 12 bits. To decode the instruction word in the system, format code (Figure 2A Element 51) will be decoded before the rest of the instruction in the word is derived (Column 8 lines 27-35). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on the combination of Fisher and Barry's inventions to incorporate Takayama's inventions. One of ordinary skill in the art would be motivated to have high degree of parallelism and efficient doe structure (Column 1 lines 55-61).

20. Claim 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fisher in view of Barry.

As per claim 15, Barry discloses:

Using an instruction address to fetch an instruction word (Column 8 lines 60-65); Executing instruction from the fetched instruction word (Column 5 lines 26-36); Controlling a way in which instruction execution is parallelized dependent on the interrupt received that switch between high/low ILP mode (Column 6 line 38-47).

Fisher does not disclose an detection unit to control the way execution unit parallelizes processing of the instruction depending on the detected range of instruction address. However, Barry discloses the above limitations (Column 1 lines 44-45), where “generalized eventpoint mechanism” is the detection unit because it allows the user to define a group of event (includes if an instruction address occurred) to detect and define a group of action (includes generating an interrupt) to take in the event of such detections (Abstract lines 4 to 15). Barry’s invention include multiple register to define multiple event(Figure 4 Element 410, Column 8 lines 15-20), also it is possible to specify a range of instruction address to generate interrupt by using mask register (Column 25 lines 5 –12).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on Fisher’s inventions to incorporate Barry’s inventions so the detection unit disclosed by Barry will detect the range of instruction address and generate interrupt according to switch between high/low ILP mode in Fisher’s invention. One of ordinary skill in the art would be motivated to include a detection unit (Barry Column 1 line 44-45) which is providing a common and flexible design for all different type of functions often needed by the processor (Column 2 lines 4-13, 33-41).

As per claim 16, the rejection of claim 15 is incorporated and Fisher further discloses:

Adapting a width of the fetched instruction word (Column 5 line 62-67 and Column 6 line 55 –63) dependent on the interrupt received that switch between high/low ILP mode (Column 6 line 38-47).

Fisher does not disclose the adjustment of width dependent on detected range of instruction address.

However, Barry discloses a detection unit. See rejection of Claim 15.

As per claim 17, the rejection of claim 15 is incorporated and Fisher further discloses: Changing a selection of functional unit of the apparatus that is used to execute the instruction (Column 5 lines 62-67, Column 6 lines 1-25, Column 7 lines 15 –36) dependent on the interrupt received that switch between high/low ILP mode (Column 6 line 38-47).

Fisher does not disclose the selection dependent on detected range of instruction address.

However, Barry discloses a detection unit. See rejection of Claim 15.

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kodama et al. (USPN 6026486) which describes a plurality of memory unit that each supply part of the instruction word, a execution unit that execute code with variable bit width. Shang et al. (USPN 5941980) which describe VLIW processor with a plurality of memory unit, execution unit that execute code in variable bit

width. Matsuo et al. (US PG Pub 2002/0133692 A1) which alter the way processor parallelize processing of instructions dependent on the instruction address.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Fong whose telephone number is 571-270-1409. The examiner can normally be reached on Monday to Thursday from 7:30 to 5:00. The examiner can also be reached on alternate Friday from 7:30 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chameli Das can be reached on 571-272-3696. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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